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2 kV slanted tri-gate GaN-on-Si Schottky barrier diodes with ultra-low leakage current

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This letter reports lateral GaN-on-Si power Schottky barrier diodes (SBDs) with unprecedented voltage-blocking performance by integrating 3-dimensionally a hybrid of tri-anode and slanted tri-gate architectures in their anode. The hybrid tri-anode pins the voltage drop at the Schottky junction (V_{SCH}), despite a large applied reverse bias, fixing the reverse leakage current (I_R) of the SBD. Such architecture led to an ultra-low I_R of 51 ± 5.9 nA/mm at −1000 V, in addition to a small turn-on voltage (V_{ON}) of 0.61 ± 0.03 V. The slanted tri-gate effectively distributes the electric field in OFF state, leading to a remarkably high breakdown voltage (V_{BR}) of −2000 V at 1 μA/mm, constituting a significant breakthrough from existing technologies. The approach pursued in this work reduces the I_R and increases the V_{BR} without sacrificing the V_{ON}, which provides a technology for high-voltage SBDs, and unveils the unique advantage of tri-gates for advanced power applications. *Published by AIP Publishing.* https://doi.org/10.1063/1.5012866

High-voltage rectifiers are crucial in nearly every topology of power converters, and GaN-on-Si Schottky barrier diodes (SBDs) are highly promising for such applications due to their superior performance and competitive cost.[1–8] Moreover, they are lateral devices and can be monolithically integrated with GaN-on-Si transistors and circuits, which is highly desirable for future compact and efficient power converters.[9,10]

Despite these advantages, a major obstacle for GaN-on-Si SBDs is their limited voltage-blocking performance. Efficient power devices must present high V_{BR} and small I_R, which are however very challenging in GaN SBDs. First, the I_R in GaN SBDs is typically large, being dominated by many non-ideal effects that are very difficult to eliminate, such as tunneling.[11] Second, although a small Schottky barrier (Φ_B) leads to a small V_{ON}, it also increases the I_R, and thus, there is a natural trade-off between good ON- and OFF-state performances. Finally, the lateral current conduction in GaN SBDs results in an inhomogeneous distribution of the electric field, which severely limits their V_{BR},[12,13] despite the resistivity of their buffer layers. Consequently, the poor voltage-blocking capability in GaN-on-Si SBDs is usually limited by the device architecture, rather than their buffer layers. As an example, the voltage-blocking performance of GaN-on-Si SBDs is still much inferior than that of GaN-on-Si transistors, even though they share the same material platform. While GaN-on-Si power transistors have been commercialized for applications up to 650 V, GaN-on-Si SBDs for such ratings are still missing.

In this work, we demonstrate that high-performance GaN-on-Si power SBDs with superior voltage-blocking capabilities (2 kV at 1 μA/mm) can be achieved with a judicious device design, by integrating hybrid tri-anode (TA) and slanted tri-gate (TG) architectures. The hybrid tri-anode reduced the I_R by controlling the V_{SCH} with the width of its nanostructures (w), resulting in an ultra-low I_R of 51 ± 5.9 nA/mm at −1000 V and in a small V_{ON} of 0.61 ± 0.03 V. The slanted tri-gate provided a continuous gradient of pinch-off voltage (V_p) from the anode towards the cathode, spreading effectively the electric field in OFF state, leading to a record V_{BR} of 2 kV at 1 μA/mm. These results establish a milestone for GaN power devices and could lead to enormous opportunities for future monolithic GaN power circuits.

The $Al_{0.25}Ga_{0.75}N$/GaN heterostructure in this work was grown on a silicon substrate with 5 μm-thick buffer layers. The fabrication of the slanted tri-gate SBDs (Fig. 1) started with e-beam lithography to define the nanostructures in the anode, which were etched by inductively coupled plasma with a depth of ∼180 nm. The width (w) and spacing of the nanostructures in the tri-gate and tri-anode regions were 200 nm and 400 nm, respectively, while the w in the slanted tri-gate region increased continuously from 200 nm to 600 nm

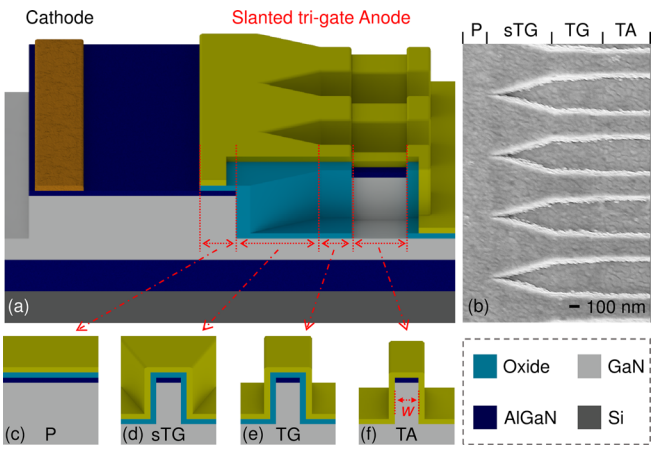

FIG. 1. (a) Schematic of the slanted tri-gate SBD and (b) a top-view scanning electron microscopy (SEM) image of the anode region. Cross-sectional schematics of the (c) planar (P), (d) slanted tri-gate (sTG), (e) tri-gate (TG), and (f) tri-anode (TA) regions comprising the anode.

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towards the cathode. The devices were isolated by mesa etching, and the cathode ohmic contact was formed by alloying Ti/Al/Ti/Ni/Au at 830 °C. Then, 10 nm SiO_2 and 10 nm Al_2O_3 were deposited by atomic layer deposition and selectively removed in the tri-anode region. Finally, the anode contact was formed with Ni/Au. The oxide in the access and ohmic regions was removed by wet etching, which did not affect the I_R in this work. The length of the planar (L_{FP}), slanted tri-gate (L_{sTG}), tri-gate (L_{TG}), and tri-anode (L_{TA}) regions was 1.3 μm, 0.7 μm, 0.5 μm, and 4 μm, respectively (Fig. 1). All current values in this work were normalized by the width of the device footprint (60 μm).

The schematic and equivalent circuit of the nanostructured anode are shown in Figs. 2(a) and 2(b), respectively. It consists of a tri-anode SBD connected in series with a tri-gate, a slanted tri-gate, and a planar-gate transistor. The main idea is to design the distribution of potential along the device in OFF state, by engineering the profile of V_p with w in a single fabrication step, to obtain small I_R and high V_{BR}. More specifically, the purpose of each component can be briefly explained as follows:

1. The tri-anode (TA) was designed for small V_{ON}[8,14] and low I_R.[15] In ON state, the metal contacts the 2DEG directly at the sidewalls and hence leads to a small V_{ON}. In OFF state, when the voltage is below the V_p of the tri-anode ($V_{p,TA}$), the V_{SCH} is pinned at $|V_{p,TA}|$ [Fig. 2(c)], which fixes the I_R at a constant level. $|V_{p,TA}|$ can be reduced continuously with smaller w [Fig. 2(d)], resulting in a smaller V_{SCH} and hence in an exponentially lower I_R, as quantified in our previous study.[15] Therefore, here the I_R is controlled by V_{SCH}, instead of by the Φ_B, so it can be reduced without sacrificing the V_{ON},[15] which decouples the I_R and V_{ON}.
2. The tri-gate region (TG) was inserted to shield the tri-anode, since the TA is vulnerable to high electric fields, which are concentrated at its cathode-side edge, and can lead to large I_R and even early breakdown of the device.[15] By connecting the TG in series with the TA, the voltage drop at the cathode-edge of the TA (V_{TA}) is pinned at $|V_{p,TG} - V_{p,TA}|$ [Fig. 2(c)], which can be also reduced with a smaller w [Fig. 2(d)], when w is below 1 μm, shielding the TA from large reverse biases. More details about the impact of the w on device characteristics can be found elsewhere.[1]
3. The slanted tri-gate (sTG) was included to enhance the V_{BR}.[16] It was patterned with a slanted w, increasing towards the cathode. Since the $|V_p|$ in a tri-gate MOS structure reduces with smaller w [Fig. 2(d)], the sTG works as many incrementally stepped field plates (FPs)[16] with a continuous gradient of $|V_{p,sTG}|$ increasing towards the cathode. As a result, the electric field is spread along the entire sTG, which significantly improves the V_{BR} [Fig. 2(c)], similarly to conventional slanted FPs, but with the advantage of a much easier and more controllable fabrication by simply tuning the w lithographically in a single step;
4. The long planar region (P) works as a planar FP to further improve the V_{BR}, since the V_p of the planar region ($V_{p,P}$)

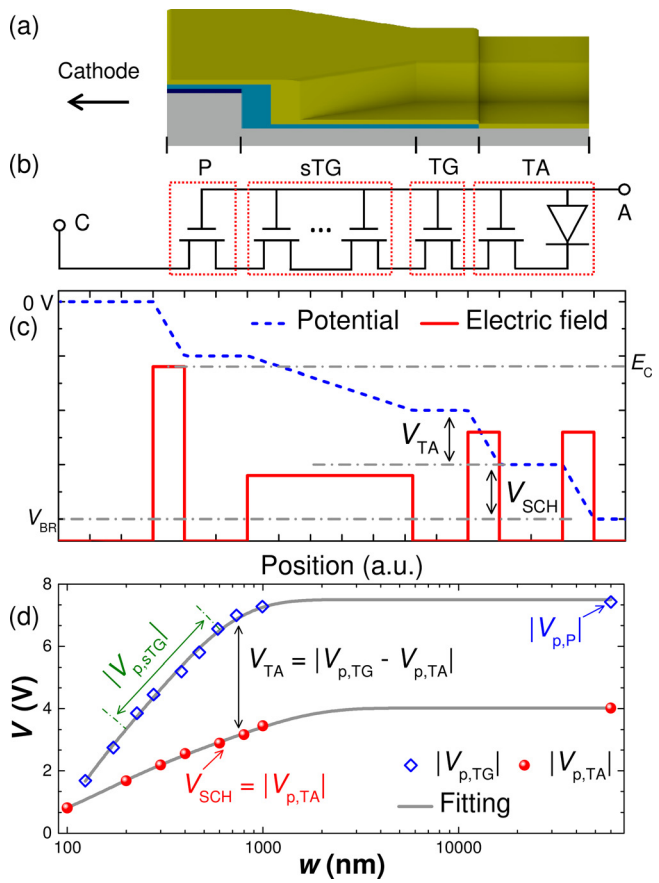

FIG. 2. (a) Schematic and (b) equivalent circuit of the slanted tri-gate SBDs. (c) Schematic showing the distribution of potential and electric field at the 2DEG channel in the SBD under a large reverse bias. (d) Averaged absolute value of the pinch-off voltage ($|V_p|$) as a function of the width (w) of the nanowires in tri-gated AlGaN/GaN structures, determined from about eight devices of the each type fabricated on a control sample with 20 nm Al_2O_3 as the oxide.

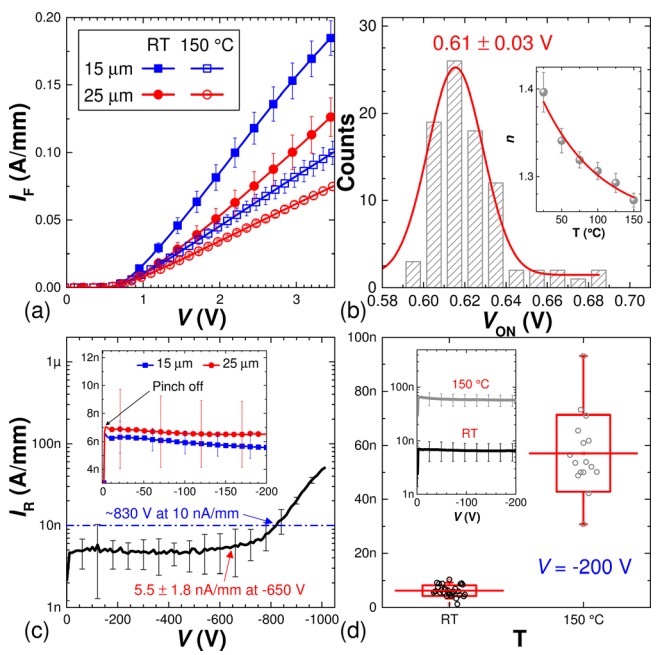

FIG. 3. (a) Forward I-V characteristics and (b) distribution of V_{ON} of the slanted tri-gate SBDs. The inset shows the dependence of the estimated ideality factor (n) upon the temperature (T). (c) Average I_R from ten devices measured at room-temperature (RT) with a floating substrate connection. The value of I_R was independent from the substrate connection when V was below −900 V. The inset shows the I_R with 15 μm and 25 μm of L_{AC} at RT. (d) I_R at RT and 150 °C measured under a voltage of −200 V. The inset shows the reverse I-V characteristics at different temperatures.

is more negative with respect to the most negative value of the $V_{p,sTG}$.[16,17]

The slanted tri-gate SBDs presented very good ON-state performance as shown in Fig. 3(a), despite the partial removal of the 2DEG in the anode. The ON-resistance (R_{ON}) was 13.9 ± 1.3 Ω mm and 22 ± 2.9 Ω mm at room temperature for devices with L_{AC} of 15 μm and 25 μm, respectively, and increased to 27.6 ± 2.9 Ω mm and 37 ± 1.8 Ω mm at 150 °C. The V_{ON} was as small as 0.61 ± 0.03 V [Fig. 3(b)], determined at 1 mA/mm. The ideality factor (n) was 1.40 ± 0.02 at room-temperature (RT) and reduced to 1.27 ± 0.01 at 150 °C [inset in Fig. 3(b)], indicating the high quality of the sidewall Schottky contacts despite the etching.

In OFF state, the I_R of the slanted tri-gate SBDs was saturated after the pinch-off of the tri-anode at about −1.7 V [the inset in Fig. 3(c)] due to the fixed V_{SCH}, which was not affected by L_{AC}, and thus, the I_R was nearly constant at 5.5 ± 1.8 nA/mm until −650 V and did not reach 10 nA/mm until −830 V [Fig. 3(c)]. Extremely low I_R of 51 ± 5.9 nA/mm was observed at −1000 V, which is significantly smaller than in any other reports of GaN-on-Si SBDs. For voltages below −900 V, there was no significant difference in I_R measured with floating and grounded substrates. From RT to 150 °C, the I_R increased by only ~50 nA/mm [inset of Fig. 3(d)], and at 150 °C, the I_R at −200 V was as small as 57 ± 13 nA/mm [Fig. 3(d)]. This is the smallest I_R among reported lateral GaN SBDs at such high temperature.

In addition to their small V_{ON} and ultra-low I_R, the slanted tri-gate SBDs also presented high V_{BR} [Fig. 4(a)]. With floating substrate, the V_{BR} at 1 μA/mm was −1450 V and −2000 V, and the hard breakdown was −1500 V and −2500 V for devices with L_{AC} of 15 μm and 25 μm, respectively, corresponding to a critical breakdown field of 1 MV/cm (extracted from the hard breakdown voltage versus L_{AC}). With grounded substrate, the V_{BR} at 1 μA/mm for both L_{AC} was about −1060 V, while the hard breakdown was up to −1200 V, which is comparable to current 650 V-rated GaN-on-Si power transistors[18–21] and is limited by the vertical breakdown of the buffer layers.[22] These results indicate that the 15 μm-L_{AC} SBDs can fulfill the voltage-blocking requirements of 600/650 V applications, even for those requiring grounded substrate connection, and the 25 μm-L_{AC} SBDs can be used for 1200 V applications (with floating substrate connection[22]) both providing a safety margin in breakdown of about 100% (from the rated voltage to the hard breakdown).

Figure 4(b) shows the C-V measurement characteristics of the slanted tri-gate SBDs plotted along with the I_R. The slanted tri-gate SBDs presented ultra-low I_R, because their V_{SCH} was pinned and the I_R saturated at the pinch-off of the tri-anode, at about −1.7 V [Fig. 4(b)], instead of increasing exponentially with the voltage. This decouples the I_R from the V_{ON}, allowing an independent design of the forward and reverse performance of the SBD, which is a major feature of this architecture. The high V_{BR} of the slanted tri-gate SBDs was due to the better-distributed electric field along the device. The continuity of the C in the slanted tri-gate region [sTG + TG region in Fig. 4(b)] indicates a gradual depletion of the channel with increasing reverse bias, due to the gradient of V_p, which spread effectively the electric field and greatly improved the V_{BR}. Such an effect is similar to conventional slant FPs[23] but obtained here with a more precise and controllable way of tuning the w lithographically, instead of the complex sloped etch of the FP oxide.

The slanted tri-gate SBDs are also promising for fast switching, due to their small capacitive charge (Q_C) of 0.263 ± 0.13 nC/A [inset of Fig. 4(b)], which is comparable to or below reported values for fast-switching GaN power SBDs on Si (0.415 nC/A)[24] and SiC (0.213 nC/A)[25] substrates. The switching time estimated from $Q_C{}^2$ was ~263 ps, which is about 25% shorter than that of conventional high-voltage GaN SBDs with double FPs.[4]

The high performance of the slanted tri-gate SBDs makes them excellent power rectifiers (Fig. 5), presenting

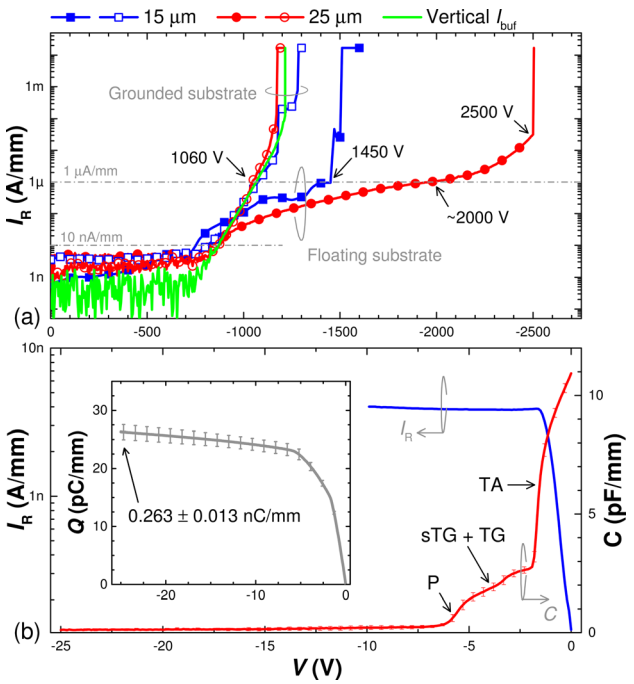

FIG. 4. (a) Breakdown characteristics of the slanted tri-gate SBDs, measured at room temperature. (b) The capacitance-voltage (C-V) characteristics of the SBDs along with their I_R. The inset shows the cumulative charge (Q_C) of the devices. The C-V measurement was performed at 1 MHz at room temperature, with negligible hysteresis observed from double-sweep measurements.

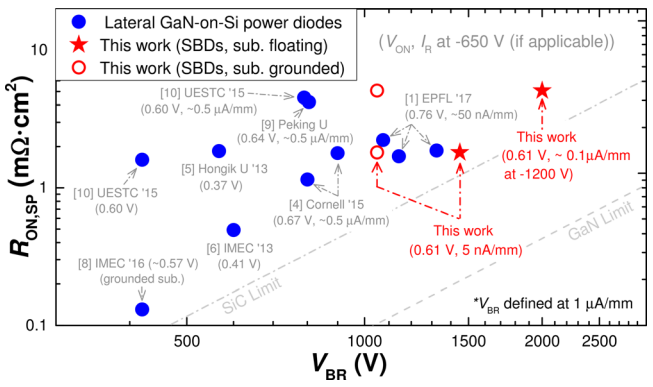

FIG. 5. Specific on-resistance ($R_{ON,SP}$) versus V_{BR} benchmark of the slanted tri-gate SBDs against state-of-the-art lateral GaN-on-Si SBDs by defining the V_{BR} at $I_R = 1$ μA/mm. The V_{BR} for all reference devices was re-calculated based on the reported data following the definition of V_{BR} at $I_R = 1$ μA/mm. For fair comparison, devices with unspecified R_{ON} or I_R were not included.

the highest V_{BR}, the lowest I_R of 5.5 ± 1.8 nA/mm at -650 V (or ~ 0.1 μA at -1200 V), a small V_{ON} of 0.61 ± 0.03 V, and an excellent high-power figure-or-merit up to 1.16 GW/cm^2, as compared with existing GaN-on-Si power diodes with conventional technologies, rendering a breakthrough for the family of GaN-on-Si power devices.

In conclusion, in this letter, we presented 2 kV GaN-on-Si power SBDs by 3-dimensional integration of slanted tri-gate and hybrid tri-anode architectures. The hybrid tri-anode allows an independent design of the forward and reverse performances of the SBD, resulting in an ultra-low I_R and a small V_{ON}. Together with the slanted tri-gate, a high V_{BR} of -2000 V at 1 μA/mm was achieved, yielding a significant breakthrough from existing technologies. The approach presented in this work demonstrates a pathway to achieve high-voltage power SBDs and opens enormous opportunities for future monolithic GaN power converters.

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